WHAT IS CLAIMED IS:

1. A method for debugging a system comprising:

1) coupling first signals to a re-writeable trace array, said trace array having M storage locations, said M storage locations having corresponding M storage addresses from a starting address to an ending address;

2) generating a first event sequence signal in response to a first sequence of occurrences of a first event signal;

3) starting, in response to said first event sequence signal, a process of storing states of said first signals sequentially in said trace array at locations beginning at said starting address and proceeding sequentially to said ending address, said process of storing states of said first signals wrapping back to said starting address when said ending address is exceeded;

4) generating a second event sequence signal in response to a second sequence of occurrences of said first event signal;

5) stopping said process of storing states of said first signals in said trace array in response to said second event sequence signal; and

6) repeating steps 2) through 5) unless stopped by a second event signal.

2. The method of claim 1, further comprising the step of:

storing an event storage address in response to receipt of said first event sequence signal, said second event sequence signal or said second event signal, said event storage address corresponding to a storage address of sub-array K which is storing states of said first signals when said first event sequence signal, said second event sequence signal or said second event signal occurred.

3. The method of claim 2, further comprising the steps of:

reading stored states of said first signals from selected storage addresses of said trace array; and

analyzing said stored states of said first signals to debug or analyze said system.

4. The method of claim 3, wherein one of said stored event storage addresses is compared to a read storage address of said trace array during reading said stored states of said first signals, a comparison match of said stored event storage address to said read storage address corresponding to event or error states of said first signals.

5. The method of claim 1, wherein said system comprises logic circuits in a very large scale integrated circuit (VLSI) chip.

6. The method of claim 5, wherein said re-writeable trace array is included within said VLSI chip.

7. The method of claim 1, wherein said first and second event signals are logic combinations of circuit states occurring within said system.

8. The method of claim 1, wherein a storage address of said trace array, corresponding to said first event sequence signal, said second event sequence signal or said second event signal, is saved.

9. The method of claim 1, wherein said first sequence of occurrences of said first event signal comprises a next sequential first event signal following a start signal.

10. The method of claim 1, wherein said second sequence of occurrences of said first event signal comprises a next sequential first event signal following said first event sequence signal.

11. The method of claim 9, wherein said second sequence of occurrences of said first event signal comprises a next sequential first event signal following said first event sequence signal .

12. An apparatus for debugging a system comprising:

a coupling circuit operable to couple first signals to a re-writeable trace array, said trace array having N storage locations, said N storage locations having corresponding N storage addresses from a starting address to an ending address;

an event sequence circuit operable to generate a first event sequence signal in response to a first sequence of occurrence of a first event signal and a second event sequence signal in response to a second sequence of occurrence of said first event signal;

a store circuit operable to stores states of said first signals in said trace array by cyclically repeating the selection of said N storage addresses from a start storage address through an Nth storage address, said store circuit starting said store of said first signals in response to said first event sequence signal and stopping said store of said first signals in response to said second event sequence signal or a second event signal; and

a read circuit operable to read contents of said trace array at selected ones of said N storage addresses.

13. The apparatus of claim 12, further comprising an address store circuit operable to store an event storage address in response to receipt of said first event sequence signal, said second event sequence signal or said second event signal, said event storage address

corresponding to a storage address of said trace array which is storing states of said first signals when said first event sequence signal, said second event sequence signal or said second event signal occurred.

14. The apparatus of claim 13, further comprising a compare circuit operable to compare one of said event storage addresses to a read storage address of said trace array during reading said stored states of said first signals, a comparison match of said event storage address to said read storage address corresponding to event or error states of said first signals.

15. The apparatus of claim 12, wherein said system comprises logic circuits in a very large scale integrated circuit (VLSI) chip.

16. The apparatus of claim 15, wherein said re-writeable trace array is included within said VLSI chip.

17. The apparatus of claim 12, wherein said first and second event signals are logic combinations of circuit states occurring within said system.

18. The apparatus of claim 12, wherein contents of said trace array at selected addresses are read out and analyzed to debug or analyze said system.

19. The apparatus of claim 12, wherein an address of said trace array, corresponding to said first event sequence signal, said second event sequence signal or said second event signal, is saved.

20. The apparatus of claim 12, wherein said first sequence of occurrences of said first event signal comprises a next sequential first event signal following a start signal.

21. The apparatus of claim 12, wherein said second sequence of occurrences of said first event signal comprises a next sequential first event signal following said first event sequence signal.

22. The apparatus of claim 20, wherein said second sequence of occurrences of said first event signal comprises a next sequential first event signal following said first event sequence signal.

23. A data processing system comprising:

a central processing unit (CPU);
random access memory (RAM);
read only memory (ROM);
an I/O adapter; and
a bus system coupling said CPU to said ROM, said RAM, wherein said CPU further comprises:

a very large scale integrated (VLSI) chip, said VLSI chip comprising a debugging system for debugging circuits within said chip said debugging system comprising;

a coupling circuit operable to couple first signals to a re-writeable trace array, said trace array having N storage locations, said N storage locations having corresponding N storage addresses from a starting address to an ending address;

an event sequence circuit operable to generate a first event sequence signal in response to a first sequence of occurrence of a first event signal and a second event sequence signal in response to a second sequence of occurrence of said first event signal;

a store circuit operable to stores states of said first signals in said trace array by cyclically repeating the selection of said N storage addresses from a start storage address through an Nth storage address, said store circuit starting said store of said first signals

in response to said first event sequence signal and stopping said store of said first signals in response to said second event sequence signal or a second event signal; and

a read circuit operable to read contents of said trace array at selected ones of said N storage addresses.

24. The data processing of claim 23, further comprising an address store circuit operable to store an event storage address in response to receipt of said first event sequence signal, said second event sequence signal or said second event signal, said event storage address corresponding to a storage address of said trace array which is storing states of said first signals when said first event sequence signal, said second event sequence signal or said second event signal occurred.

25. The data processing of claim 24, further comprising a compare circuit operable to compare one of said event storage addresses to a read storage address of said trace array during reading said stored states of said first signals, a comparison match of said event storage address to said read storage address corresponding to event or error states of said first signals.

26. The data processing of claim 23, wherein said system comprises logic circuits in a very large scale integrated circuit (VLSI) chip.

27. The data processing of claim 26, wherein said re-writeable trace array is included within said VLSI chip.

28. The data processing of claim 23, wherein said first and second event signals are logic combinations of circuit states occurring within said system.

29. The data processing of claim 23, wherein contents of said trace array at selected addresses are read out and analyzed to debug or analyze said system.

30. The data processing of claim 23, wherein an address of said trace array, corresponding to said first event sequence signal, said second event sequence signal or said second event signal, is saved.

31. The data processing of claim 23, wherein said first sequence of occurrences of said first event signal comprises a next sequential first event signal following a start signal.

32. The data processing of claim 23, wherein said second sequence of occurrences of said first event signal comprises a next sequential first event signal following said first event sequence signal.

33. The data processing of claim 32, wherein said second sequence of occurrences of said first event signal comprises a next sequential first event signal following said first event sequence signal.